ISSN: 0974-2115
www.jchps.com Journal of Chemical and Pharmaceutical Sciences

A New Approach to Reduce Leakage Current in 6t SRAM Using Finfet

S. Beulah Hemalatha, M. Jasmin, Bibhuti Bhusan Mahapatra
Department of ECE, Bharath university
***Corresponding author: E-Mail: Beulah_s@gmail.com**

ABSTRACT

Over the past decades, the VLSI designers mainly concentrated on performance and miniaturization. But with the growth in wireless communication and portable computing, power dissipation has become a critical issue. The magnitude of power dissipated per unit area also grows with scaling. The computational performance requirement of the portable applications is similar to that of the non-portable ones. Increased battery life becomes very important. Because of these factors, power dissipation becomes extremely important for circuit designers and also critical issue in the microelectronics industry. This project represents the simulation of different SRAM cell and their comparative analysis on different parameters such as power supply and area efficiency etc. All the simulation has been carried out on 45nm at tanner EDA tool.

KEY WORDS: SRAM cell, miniaturization, computational performance.

1. INTRODUCTION

An integrated circuit is composed by sequential and combinational circuits, memories blocks and I/O devices. There are four components of power dissipation in digital CMOS circuits is shown in Fig.1

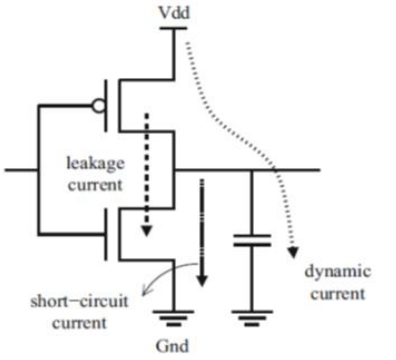


Figure.1. Power Dissipation

$$P = P_{DymanicSwitching} + P_{shortcircuit} + P_{Staticbiasing} + P_{Leakage} \quad (1)$$

Dynamic power dissipation: Dynamic power dissipation occurs during the capacitance charging and discharging in the circuit. At each rising edge of the output transition, PMOS transistor charges the load capacitance C_L, and a some part of energy is taken from the power supply. A small portion of the energy gets dissipated in PMOS circuit and some portion gets stored on C_L. This stored energy gets discharged during the negative edge of the output transition, and the stored energy is lost through the NMOS transistor.

Short circuit power dissipation: Short–circuit power is another important source of power dissipation. When any input signal changes, for a short interval both the transistors become ON and conduct together. This causes a dc current flow via the direct path that exists between the ground and the dc power supply.

Leakage power dissipation: The transistors employed in a CMOS logic circuit generally have nonzero reverse leakage current and subthreshold current. These current also adds up to total power dissipation even when the transistors are not doing any switching operation. Leakage current mainly depend on.

- Leakage current at the junction under Reverse-biased condition (*IREV*)
- Gate induced drain leakage (*IGIDL*)
- Gate direct-tunnelling leakage
- Sub-threshold leakage Current (*ISUB)*

Existing Technique

Conventional 6T SRAM cell: Every bit in a SRAM is gets stored on four transistors that frame two cross-coupled inverters. 0 and 1 represents the two stable states of the storage cell. During read and write operations, storage cell access can be controlled by two additional transistors. A SRAM cell generally requires six MOSFETs to store each memory bit. Access to the cell is empowered by the word line. This word line controls the two access transistors M5 and M6 which, thusly, control whether the cell ought to be associated with the bit lines: BL and BL bar. They are utilized to exchange information for both read and write functionalities.

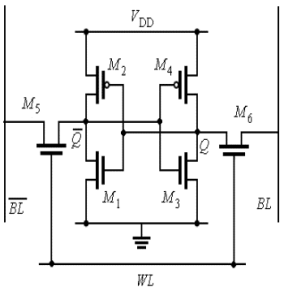


Figure.2. Conventional 6T SRAM Cell

An SRAM cell has three different states it can be in: standby state or idle state, reading state when the data has been requested and writing state when updating the contents. The SRAM to work in read mode and write mode must have "readability" and "write stability" respectively.

Proposed Technique

6T SRAM Design Using FinFET

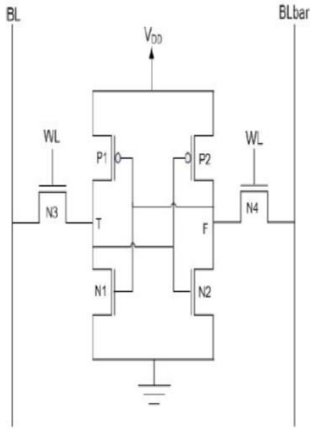


Figure.3. 6T SRAM using FinFET

The double gate FinFET SRAM cell a is good choice because of the self-alignment of the two opposite side of gates. Its fabrication technology is highly adaptable with the conventional CMOS fabrication technology. The leakage can be reduced by changing the supply voltage (Vdd), fin height and threshold voltage (Vth). When the Fin-height is increased it causes decrease in Vdd, but reduction in Vdd affects the stability of the SRAM cell. Memories with high speed and low power dissipation are needed. Hence FinFET based SRAM cells have the advantage of low power dissipation. Also, FinFET cell provides higher noise margins. FinFET offers good control over the short-channel effects without reducing the width of the gate-oxide and increasing the density of channel doping. It operates in the following ways: shorted or tied gate (SG) mode, low power (LP) mode, and independent gate (IG) mode, and IG/LP mode. In the IG mode, both the gates are controlled to reduce the power consumption.

Simultaneously Driven Double Gate: Shorted gate FinFET SRAM comprises of WL to empower access FinFET NMOS transistors. A bulk CMOS SRAM can be formed by associating two individual FinFET inverters. FinFET decreases the short channel effect and thus decreases leakage. Be that as it may, the delay increments in the 6T SRAM by utilizing DG FinFET to a certain degree throughout the read and write cycle. Minimum sized transistors are considered in this paper. Minimum sized SRAM offers good noise immunity and dependability, least estimated SRAM is profoundly attractive, however the upgrade in solidness through SRAM sizing, includes some major disadvantages of increased leakage power consumption and cell area.

Independent Driven Double Gate: In the independent gate DG FinFET opposite side of the two gates are kept separated from each other. Each gate is biased independently which allows multiple threshold voltages. This helps in reducing the transistor count. Independent gate DG

SRAM cell is structured in such a way that leakage current gets reduced .This increases the stability and the performance of the cell will be increased. Fins should be of minimum width. The alternate gates in pull up transistors can be controlled individually in the cross coupled inverters. Alternate gates in pull down transistors can be connected to one another and this provides multiple threshold voltage.

When *Vt* is smaller than a potential voltage, the current flow between drain to source gets activated by the gates of the double gate or FINFET device, by channel modulation from two sides instead of one side. The potential of the channel gets influenced by the potential which is applied to the two gates. This potential fights against the drain impact and gives the better shut off to the channel current and hence lowers reduces Drain Induced Barrier Lowering (DIBL). The FINFET model structure can be divided into following regions.

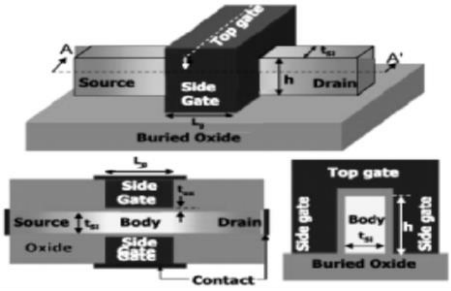


Figure.4. FinFET model structure

- silicon fin with less doping
- poly-silicon region with heavy doping
- contact region between source and drain –heavily doped
- Gate oxide region (SiO2)

FINFET device modeling parameter: The FINFET is basically called the folded channel MOSFET. It has narrow vertical fins from the wafer. The gate width will be twice the height of the fin in FINFETs. FINFETs are preferred instead of CMOS in below 45nm technology because effective manufacturing cost is less. The geometric key attributes of FINFETs are

i. L_g - Gate length,
ii. h – Fin Height,
iii. t_{ox}- gate oxide Thickness,
iv. t_{ox-top} - Top gate Oxide thickness and fin thickness,
v. T_{si}- Fin thickness
vi. Doping of the Channel.

These attributes play a vital role in reducing the I_{off} leakage current and helps to increase the I_{on}current.

Reduction of I_{off}: The drain current when V_{gs} = 0 V and $V_{ds} = V_{dd}$ is termed as I_{off} .

Under ideal case, I_{off} = 0.

Sources of I_{off}

- Thermionic emission (main)
- Quantum Mechanical Tunneling
- Band-to-Band Tunneling

When we move anybody away from the control of the gate, I_{off} gets increased. When we place another gate on the flip side of the device, this doubles the gate channel capacitance and the channel potential comes under the gate electrode control, this reduces the value of I_{off}.

- Minimizing the body thickness further reduces I_{off}.
- Minimizing the body thickness inturn increases series resistance Rr=L/A.
- A raised source/drain structure can be used to reduce the series resistance.

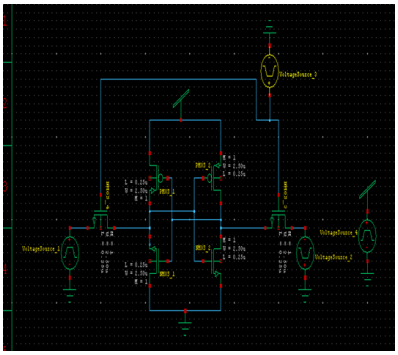
Devices parameter used in simulation: In HSPICE simulation 45nm gate length FinFET technology were used for the transistors in the SRAM cells. Simulation is carried out for both symmetrical and independent double gate FinFET.

Table.1. Devices parameter

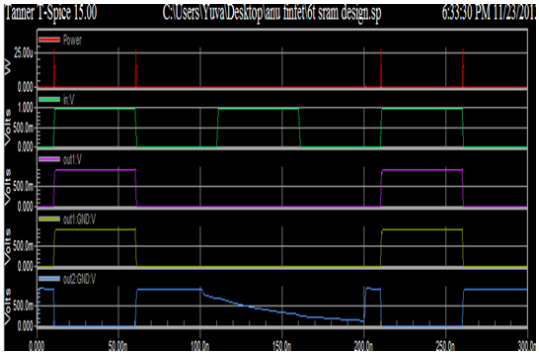
$L_G(nm)$	45
$T_{ox}(A)$	15
$T_{si}(nm)$	8.4
$V_{DD}(V)$	1
$N_{body}\ cm^{-3}$	2e16
$H_{fin}(nm)$	60
$V_{to,}nmos(V)$	.31
$V_{to,}pmos(V)$	-0.25

2. RESULTS AND CONCLUSION

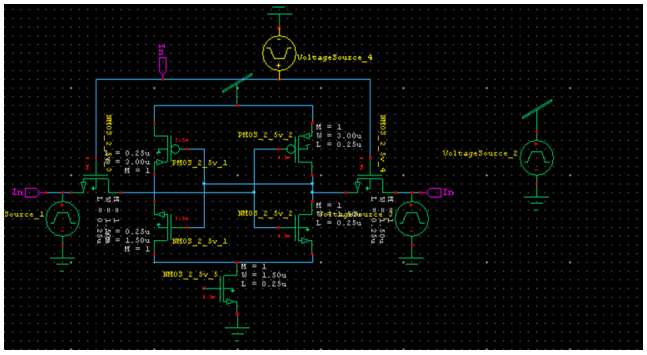
Conventional 6t Sram Using FinFET:



WAVEFORM



Independent gate



5.3.1 WAVEFORM

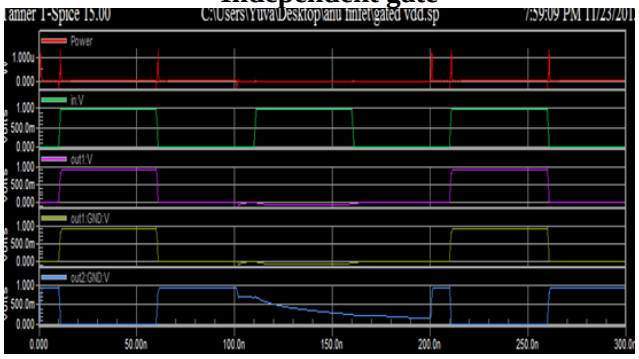


Table 5.1 Power and delay calculation

Comparison of Both Modes

Table.2. Comparison of Both Modes

S. No	Technique	Power	Delay
1	Shorted gate mode SRAM design	1.095866e-021	50ns
2	Independent gate mode SRAM design	6.301499e-022	50ns

Comparison Chart

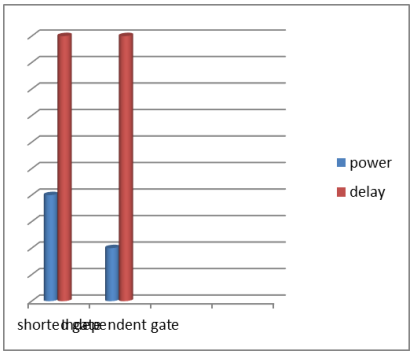


Figure.6. Comparison of power and delay

3. CONCLUSION

FinFETs are an altenative for bulk CMOS for overcoming the difficulties being postured by the scaling of conventional MOSFETs. Because of its double-gate structure, it provides inventive circuit design styles. A robust and low power 6T SRAM cell based on FinFET has been proposed in this work. These SRAM cells incorporate the uses of the Vt-control technique to the various transistors together with the inherent cell feedback. The effectiveness of these SRAM cells were tested using the TSPICE simulations with 45nm technologies. Compared with the past work on CMOS SRAM, the proposed scheme consumes low power and read access time is also low. It also provides better Static Noise Margin.

REFERENCES

Akashe S, Khandelwal S, Supply Voltage Minimization Techniques for SRAM Leakage Reduction, Journal of Computational and Theoretical Nanoscience, 9(8), 2012, 1044-1048.

Alamgir Hossain Md, Mahfuzul Haque Chowdhury, Mahfuzul Haque Chowdhury, Md Saiful Islam, Zakir Hossain M, Electrical Characteristics Of Trigate Finfet, 11(7), 2011.

Alouni A, Rjoub A, An Efficient Approach to Calculate Leakage Current Based on SPICEs Parameters at CMOS Transistors, Computer Engineering Dept, Jordan University of Science and Technology, Jordan.

Anjana R, Ajay Kumar Somkuwar, Minimizing the sub threshold for high performance CMOS circuits using novel stacked sleep transistor technique, IJEETC, 1(1), 2012.

Chauhan R.K, Sushil Kumar Gupta, Low power analysis of various 1-bit SRAM cell using spice, IJARECE, 2(8), 2013.

Ching-Te Chuang, Rajiv V, Joshi Keunwoo Kim, Koushik K, Das, Nanoscale CMOS Circuit Leakage Power Reduction by Double-Gate Device, 2004.

Devisuriya M, Logeshwari N, Sathya D, Modeling and simulation of FinFET SRAM for nanoscale devices, TIJCSA, 2(3), 2009.

Gopalakrishnan K, Sundar Raj M, Saravanan T, Multilevel inverter topologies for high-power applications, Middle - East Journal of Scientific Research, 20(12), 2014, 1950-1956.

Jasmin M, Vigneshwaran T, Beulah Hemalatha S, Design of power aware on chip embedded memory based FSM encoding in FPGA, International Journal of Applied Engineering Research, 10(2), 2015, 4487-4496.

Kanniga E, Selvaramarathnam K, Sundararajan M, Kandigital bike operating system, Middle - East Journal of Scientific Research, 20(6), 2014, 685-688.

Kanniga E, Sundararajan M, Modelling and characterization of DCO using pass transistors, Lecture Notes in Electrical Engineering, 86(1), 2011, 451-457.

Karthik B, Arulselvi, Noise removal using mixtures of projected gaussian scale mixtures, Middle - East Journal of Scientific Research, 20(12), 2014, 2335-2340.

Karthik B, Arulselvi, Selvaraj A, Test data compression architecture for low power vlsi testing, Middle - East Journal of Scientific Research, 20(12), 2014, 2331-2334.

Karthik B, Kiran Kumar T.V.U, Authentication verification and remote digital signing based on embedded arm (LPC2378) platform, Middle - East Journal of Scientific Research, 6(5), 2014, 2341-2345,

Karthik B, Kiran Kumar T.V.U, EMI developed test methodologies for short duration noises, Indian Journal of Science and Technology, 6(5), 2013, 4615-4619.

Karthik B, Kiran Kumar T.V.U, Vijayaragavan P, Bharath Kumaran E, Design of a digital PLL using 0.35Î¼m CMOS technology, Middle - East Journal of Scientific Research, 18(12), 2013, 1803-1806.

Manish Dev Singh, Shyam Akashe and Sanjay Sharma, Leakage power reduction techniques of 45 nm static random access memory (SRAM) cells, International Journal of the Physical Sciences, 6(32), 2011, 7341 – 7351.

Manorama, Saurabh Khandelwal and Shyam Akashe, Design of a FinFET Based Inverter Using MTCMOS and SVL Leakage Reduction Technique, ITM University, Gwalior, India.

Philomina S, Karthik B, Wi-Fi energy meter implementation using embedded linux in ARM 9, Middle - East Journal of Scientific Research, 6(5), 2014, 2434-2438.

Saravanan T, Sundar Raj M, Gopalakrishnan K, Comparative performance evaluation of some fuzzy and classical edge operators, Middle - East Journal of Scientific Research, 20(12), 2014, 2633-2633.

Saravanan T, Sundar Raj M, Gopalakrishnan K, SMES technology, SMES and facts system, applications, advantages and technical limitations, Middle - East Journal of Scientific Research, 20(11), 2014, 1353-1358.

Saurabh Khandelwal, Shyam Akashe, Vandna Sikarwar, Analysis of Leakage Reduction Techniques in Independent Gate DG FinFET SRAM Cell, ITM University, Gwalior, India.

Vijayaragavan S.P, Karthik B, Kiran Kumar T.V.U, A DFIG based wind generation system with unbalanced stator and grid condition, Middle - East Journal of Scientific Research, 20(8), 2014, 913-917.

Vijayaragavan S.P, Karthik B, Kiran Kumar T.V.U, Effective routing technique based on decision logic for open faults in fpgas interconnects, Middle - East Journal of Scientific Research, 20(7), 2014, 808-811.

Vijayaragavan S.P, Karthik B, Kiran Kumar T.V.U, Privacy conscious screening framework for frequently moving objects, Middle - East Journal of Scientific Research, 20(8), 2014, 1000-1005.